REMARKS

Claims 23-25 have been cancelled. Claims 26 and 27 have been added. Therefore, claims 1-22 and 26-27 are currently pending in the application. Claims 1-14 have been amended. The amendments to claims 2-14 have been made solely to comply with U.S. practice. In view of the following remarks, Applicants respectfully request forwarding of the application on to issuance.

Drawing Objections

The Office objects to Figure 8 for including reference characters not mentioned in the description. Applicants believe the Office meant to refer to Figure 7. Figure 7 has been amended to remove reference characters 100 and 102 not found in the specification.

Claim Objections

The Office objects to claim 13 for the use of the acronym "VLIW" and requests that Applicants indicate in the claim the meaning of the acronym. Applicants have amended claim 13 as requested and ask that the objection be withdrawn.

The 35 U.S.C. § 102 Rejections

Claims 1-22 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,367,067 to Odani et al (hereinafter "Odani").

Claims 1-14 and 26-27

As amended, claim 1 recites a process for executing programs on a multiprocessor system having a plurality of processors, having a given instruction set architecture. The process comprises compiling, at least in part, the instructions of the programs as instruction words of given length executable on a first processor of the plurality. The process further comprises modifying, during runtime of a program, at least some of the instruction words of given length of the program by converting them into modified-instruction words executable on a second processor of the plurality, the modification operation in turn having at least one operation

selected from the group of splitting the instruction words into modified-instruction words; and entering in the modified-instruction words no-operation instructions.

Odani does not disclose the claimed subject matter. For example, Odani does not teach modifying, ***during runtime***, at least some instructions words of given length executable on a first processor of a plurality of processors and converting them into modified-instruction words executable on a second processor of the plurality. Rather, Odani simply teaches a compiler to translate and link a source program written in a high-level language to generate an executable program for a VLIW processor. As is well known, such a compiler operates prior to, rather then during, the runtime of a program. Therefore, Odani cannnot perform any acts during ***runtime*** of the executable program.

Accordingly, for at least this reason, this claim is allowable.

Claims 2-14 and 26-27 depend from claim 1 and, as such, are allowable as depending from an allowable base claim. These claims are also allowable for their recited features which, in combination with those recited in claim 1, are neither shown nor suggested by the references as cited and applied by the Office.

Claims 15-18

Claim 15 recites a system comprising a plurality of processors coupled for receiving instruction sets. A first processor of the plurality is coupled to each of the other processors within the plurality and receives from the other processors data representative of the workload of each of the other processors. The system also comprises an output signal from the first processor to the instruction set stream. The output signal controls the instructions, which are sent to each of said processors based on the results of the workload measurement of said processors.

Odani does not disclose the claimed subject matter for at least two reasons. First, Odani does not even teach a plurality of processors. Rather, Odani simply teaches a compiler to translate and link a source program written in a high-level language to generate an executable program for a single VLIW processor. Applicants have thoroughly reviewed the Odani reference and can find no indication that Odani's system includes a plurality of processors, nor does Odani

provide any disclosure as to how his compiler would utilize more than one processor. The Office points to elements 100 and 102 in Odani's Figure 1 as disclosing a plurality of processors. However, neither 100 nor 102 even *suggest* using multiple processors. Odani's element 100 is a target processor. Nowhere does Odani suggest having more than one target processor. In fact, throughout the disclosure, Odani refers to a single target processor. Odani's element 102 is an instruction register, which is shown in Figure 1 as storing 3 instructions. Clearly an instruction register storing 3 instructions is not the same as a plurality of ***processors***. Second, because Odani does not teach a system comprising a plurality of processors, Odani cannot possibly disclose a first processor receiving workload data from other processors.

Accordingly, for at least these reasons, this claim is allowable.

Claims 16-18 depend from claim 15 and, as such, are allowable as depending from an allowable base claim. These claims are also allowable for their recited features which, in combination with those recited in claim 15, are neither shown nor suggested by the references as cited and applied by the Office.

Claims 19-22

Although the language of claims 19-22 is not identical to that of claim 15, the allowability of claims 19-22 will be apparent in view of the above discussion of claim 15.

Conclusion

Applicants respectfully submit that all pending claims are in condition for allowance. Accordingly, Applicants request that a Notice of Allowance be issued. If the Office's next anticipated action is to be anything other than a Notice of Allowance, Applicants request that the undersigned be contacted for scheduling a telephone interview.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

Respectfully submitted,

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